ABSTRACT OF THE DISCLOSURE

An apparatus for avoiding a deadlock condition in a microprocessor with a speculative branch target address cache (BTAC) that predicts a target address of a branch instruction contained in a cache line output by an instruction cache in response to a fetch address is disclosed. The BTAC incorrectly predicts the branch instruction is wholly contained in the cache line; consequently, the microprocessor fetches from the target address without fetching the next sequential cache line containing the rest of the instruction. An instruction formatter detects the instruction is only partially contained in the cache line and waits for the next cache line. However, the formatter receives no more cache lines because the target address misses in the cache and the missing cache line is not fetched from memory because the processor does not generate speculative instruction fetches. To avoid deadlocking, the apparatus invalidates the BTAC target address and retries.